REMARKS/ARGUMENTS

This Amendment is being submitted in response to the Office Action dated March 1, 2005. This Amendment is being submitted within the period for response extending to June 1, 2005.

Claims 1, 6-9, 13-14, 20, and 25-26 are currently amended.

Claims 12 and 24 are cancelled.

Claims 1-11, 13-23, and 25-29 remain pending in this case after entry of this Amendment.

Allowable Subject Matter

The Applicants acknowledge the Office's indication that claims 13, 14, 18, 25, 26, and 28 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, 2nd paragraph and to include all of the limitations of the base claim and any intervening claims.

Specification

The Office has objected to the specification based on the assertion that "pull down logic 221" as described in paragraph [0028] is misleading. The Office asserts that circuit 221 is a latch rather than pull down logic.

The Applicants respectfully disagree with the Office's assertion that circuit 221 is a latch. Figure OA1 below shows a gated latch as known to those skilled in the art. Additionally, Figures OA2 through OA4 show the transistor level schematic of the inverter, AND gate, and NOR gate used to define the gated latch in Figure OA1, as known to those skilled in the art. The gated latch of Figure OA1 functions as follows:

- When E=1, signals b and d correspond to the value of D and D', respectively. When E=1, two situations can occur:
    - If b=1 and d=0, then c=0 and Q=1; and
    - If b=0 and d=1, then c=1 and Q=0.

  In both situations, Q=D.
- When E=0, b=d=0 and the loop is used to store the value of Q.

The above-described gated latch represents one embodiment of a latch, as known to those skilled in the art. However, it should also be appreciated that other types of latches are of comparable complexity. A latch is not defined simply by two cross-coupled NMOS devices. Furthermore, a latch is required to store the state of a digital signal. The pull down logic 221 of the present invention is not defined to store the state of a digital signal. Based at least on the above discussion, the pull down logic 221 of the present invention is not a latch.

The functionality of the pull down logic 221 is described in the following excerpt from paragraph [0028] of the specification:

> "The inputs of NMOS devices M1 and M2 are connected to sense nodes SN and SN_l, respectively. However, the gates of NMOS devices M1 and M2 are connected to sense nodes SN_l and SN, respectively. Thus, as sense node SN_l begins to attain a higher state relative to sense node SN, NMOS device M1 will begin to transmit causing the state of SN to become lower. Conversely, as sense node SN begins to attain a higher state relative to sense node SN_l, NMOS device M2 will being to transmit causing the state of SN_l to become lower. Therefore, NMOS devices M1 and M2 serve to pull down sense nodes SN and SN_l, respectively, as the complementary sense node begins to attain a higher state."

In accordance with the description of the pull down logic 221 in paragraph [0028], it should be appreciated that the term "pull down logic" provides a clear and precise description of the cross-coupled NMOS devices M1 and M2 and their configuration in the sense stage 205 of the sense amplifier 201. The Office is respectfully reminded that the Applicants are entitled to be their own lexicographer. Furthermore, because the ordinary meaning of latch, as known to those skilled in the art, is not that of a cross-coupled pair of NMOS devices as described for the pull down logic 221, use of the term "latch" as suggested by the Office would be misleading and incorrect.

In view of the foregoing, the Applicants do not believe it is appropriate to change the term "pull down logic 221" to "latch" as suggested by the Office. Therefore, the Office is respectfully requested to withdraw the objection to the specification associated with use of the term "pull down logic 221."

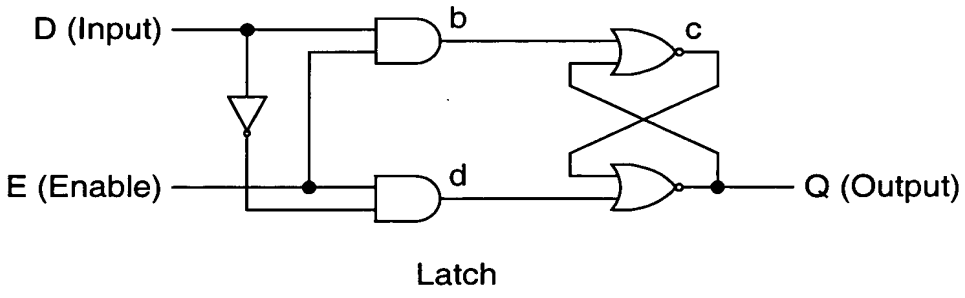

Figure OA1

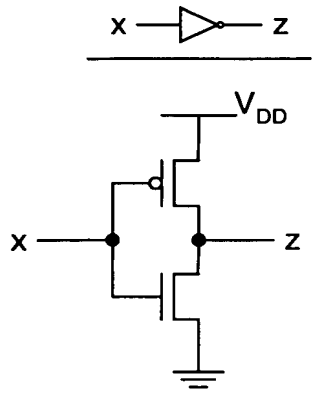

Figure OA2

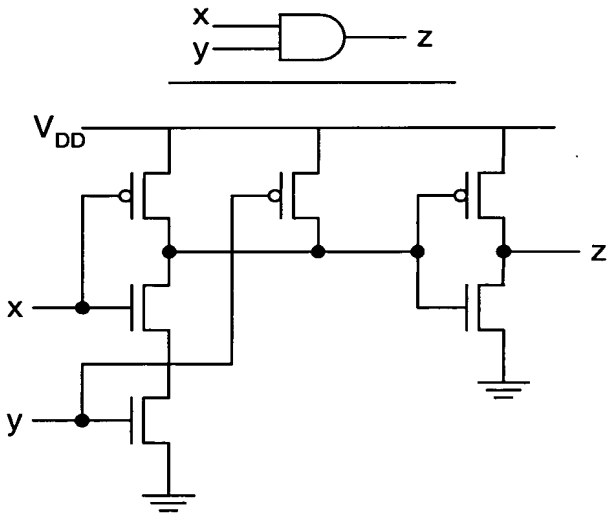

Figure OA3

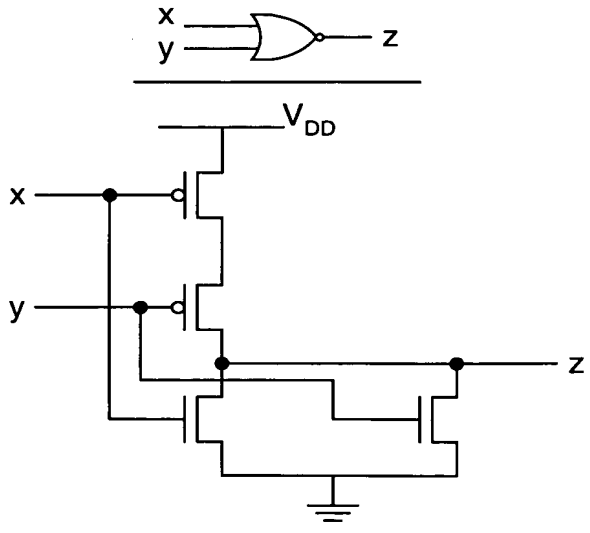

Figure OA4

Rejections under 35 U.S.C. 112

Claims 1-29 have been rejected under 35 U.S.C. 112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These rejections are traversed.

With respect to claim 1, the Office has asserted that the meaning of the phrase "higher signal" is unclear. The Office has also asserted that it is unclear how the "pair of balanced isolation devices" can provide a "higher signal."

Claim 1 has been amended to clarify that the sense stage includes a pair of sense nodes connected to receive respective output signals from the pair of balanced isolation devices of the input stage. Amended claim 1 also recites that the sense stage is further configured to amplify a voltage of the received output signal having the higher voltage. In view of the above-described clarifying amendments to claim 1, the Applicants submit that claim 1 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph.

With respect to claims 9, 19, 20, and 29, the Office has asserted that the recitation "pull down logic" in claims 9 and 19, and the recitation "pull down circuitry" in claims 20 and 19, are indefinite as being misdescriptive. The Office further asserts that the pull down logic 221 in Figure 2B is only a latch.

The Applicants disagree with the Office's assertion that the pull down logic/circuitry of claims 9, 19, 20, and 29 is equivalent to a latch. The Office is referred to the Specification section above for the Applicants arguments against the Office's assertion that the pull down logic/circuitry is only a latch. Based on the description of the pull down logic as provided in paragraph [0028] of the specification as originally filed, the pull down logic does in fact operate as such. In view of the arguments referenced above, the Applicants submit that each of claims 9, 19, 20, and 29 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph.

Furthermore, the Office's assertion that the cross-coupled NMOS devices M1 and M2 of the pull down logic 221 is equivalent to a latch has been made without supporting evidence in the cited art of record. Thus, the Office's assertion that the pull down logic 221 is equivalent to a latch is considered by the Applicants to be taken under official notice. Therefore, the Applicants hereby traverse the Office's assertion of official notice with regard to the pull down logic 221. Additionally, the Applicants request that the Office provide specific factual findings and concrete evidence in the record to support the findings with regard to the Office's position of official notice as discussed above.

With respect to claim 14, the Office has asserted that the charging devices will not supply a voltage to the input nodes when the charging devices are not enabled. The Office is requested to note that claim 14 has been amended to recite "a pair of charging devices each being configured to supply a steady voltage to a separate one of the pair of input nodes upon receipt of a recovery activation signal." The Applicants submit that amended claim 14 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph.

With respect to claim 26, the Office has asserted that "connecting an output of each of a second pair of PMOS devices to a separate one of the pair of input nodes" is indefinite because it is not clear what the "second pair of PMOS devices" is in the drawing (Figure 2B). Claim 26 has been amended to change "a second pair of PMOS devices" to "a pair of PMOS devices." When considering the combination of claims 20 and 26, the phrase "pair of PMOS devices" is clear with respect to the circuitry represented in Figure 2B. More specifically, the entities of claims 20 and 26 are depicted in Figure 2B as follows:

a pair of input nodes (inp1, inp2),

a pair of differential input signals (IN, IN_I),

a pair of balanced isolation devices (T3, T4),

a pair of sense nodes (SN, SN_I),

a common bias voltage (gp_I),

a transmission gate (215),

pull down circuitry (221), and

a pair of PMOS devices (M6, M7).

Thus, the Applicants submit that amended claim 26 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph.

In view of the foregoing, the Applicants submit that each of claims 1-29 particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Therefore, the Office is requested to withdraw all rejections under 35 U.S.C. 112, 2nd paragraph.

Rejections under 35 U.S.C. 102

Claims 1-4, 6-16, 19-24, and 29 were rejected under 35 U.S.C. 102(b) as being anticipated by McClure (U.S. Patent No. 5,455,802). These rejections are traversed.

In the *Claim Rejections-35 USC §102* section of the Office Action dated March 1, 2005, the Office indicates that claims 13-15 are rejected under 35 U.S.C. 102(b). However, claims 13 and 14 are indicated as being objected to in the Allowable Subject Matter section of the Office Action. Because the Office has not provided a basis for rejecting of claims 13 and 14 under 35 U.S.C. 102(b), the Applicants will consider claims 13 and 14 as being objected and not rejected under 35 U.S.C. 102(b). Also, the Office Action does not provide a basis for rejecting claim 15 and does not identify claim 15 as being an objected claim. However, because claim 15 depends from claim 14, which is an objected claim, the Applicants will consider claim 15 as being objected and not rejected under 35 U.S.C. 102(b).

The Office has asserted that the sense amplifier as depicted in Figure 2 of McClure teaches each and every element of the present invention. Before discussing how the presently claimed invention distinguishes over the sense amplifier of McClure, the Applicants consider it appropriate to correct several aspects of the Office's interpretation of McClure's sense amplifier.

The Office has referred to PMOS devices 28, 30, and 32 of McClure as representing part of a sense stage. However, according to McClure, PMOS devices 28, 30, 32 are only activated in response to a low equalization signal. Also, McClure states that the equalization signal is maintained in a high state during sensing on the nodes 42 and 44. Thus, PMOS devices 28, 30, 32 are not part of a sense stage.

The Office has also stated that output signals from the input stage of McClure (devices 34 and 36) are amplified by a recovering stage represented by PMOS devices 28 and 32. However, as indicated above, the PMOS devices 28 and 32 are only activated in response to a low equalization signal. During sensing, the equalization signal is high, thus the output signals from the input stage of McClure (devices 34 and 36) are not amplified or affected by the PMOS devices 28 and 32.

Claim 1 has been amended to recite that the sense stage includes a pair of booster circuits. The booster circuits are described with respect to items 217 and 219 in the specification of the present invention. Claim 1 has been amended to further recite that each of the pair of booster circuits is configured to assist in a low-to-high state transition of a separate one of the pair of sense nodes during a sensing operation. The above noted amendments to claim 1 are similar to the features recited in previously pending claim 8, which is now amended to recite features of the pair of booster circuits. The Office has referred to devices 28 and 32 of McClure as teaching the pair of booster circuits as currently recited in amended claim 1 and as recited in previously pending claim 8.

The Applicants submit, however, that devices 28 and 32 of McClure do not teach the booster circuits as presently claimed. More specifically, during a sensing operation, the equalization signal of McClure is high (column 3, lines 24-32). Therefore, the PMOS devices 28 and 32 of McClure are turned off/disabled during the sensing operation. Consequently, it is not possible that the PMOS devices 28 and 32 of McClure teach the pair of booster circuits as presently claims, wherein each of the pair of booster circuits is configured to assist in a low-to-high state transition of a separate one of the pair of sense nodes during a sensing operation.

Independent claims 9 and 20 have each been amended to also include recitation of a pair of booster devices configured to assist a low-to-high state transition of a respective one of the pair of sense nodes during a sensing operation. The Applicants submit that the pair of booster devices as recited in each of claims 9 and 20 is not taught by McClure for at least the same reasons as previously discussed with respect to claim 1.

In view of the foregoing, McClure fails to teach each and every feature of currently pending independent claims 1, 9, and 20, as required to support a rejection under 35 U.S.C. 102. Therefore, the Applicants respectfully request the Office to withdraw the rejections of claims 1, 9, and 20. Furthermore, because each of dependent claims 2-4, 6-8, 10-11, 16, 19, 21-23, and 29 ultimately depends from one of independent claims 1, 9, and 20, and incorporates all features of its respective independent claim, the Applicants submit that each of dependent claims 2-4, 6-8, 10-11, 16, 19, 21-23, and 29 is patentable for at least the reasons provided for its respective independent claim. Therefore, the Applicants respectfully request the Office to withdraw the rejections of dependent claims 2-4, 6-8, 10-11, 16, 19, 21-23, and 29.

Rejections under 35 U.S.C. 103

Claims 5, 17, and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over McClure. These rejections are traversed.

Because each of dependent claims 5, 17, and 27 ultimately depends from independent claims 1, 9, and 20, respectively, and incorporates all features of its respective independent claim, the Applicants submit that each of dependent claims 5, 17, and 27 is patentable for at least the reasons provided above for its respective independent claim. Therefore, the Applicants respectfully request the Office to withdraw the rejections of dependent claims 5, 17, and 27.

In view of the foregoing, the Applicants submit that claims 1-11, 13-23, and 25-29 are in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP383). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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